A²SI-Lite 14 / A²SI-Lite 16

Application Note
Advanced AS-Interface IC

1 Features

- Actuator-Sensor Interface (AS-i) is the simplest automation networking solution.
- AS-Interface is the ideal choice for networking sensors and actuators in factory automation and process control environments.
- AS-Interface is best seen as a digital replacement for traditional cable tree architectures.
- It is especially suitable for lower levels of plant automation where simple (often binary) field devices, such as switches, need to communicate in a stand-alone local area automation network controlled by PLC or PC.

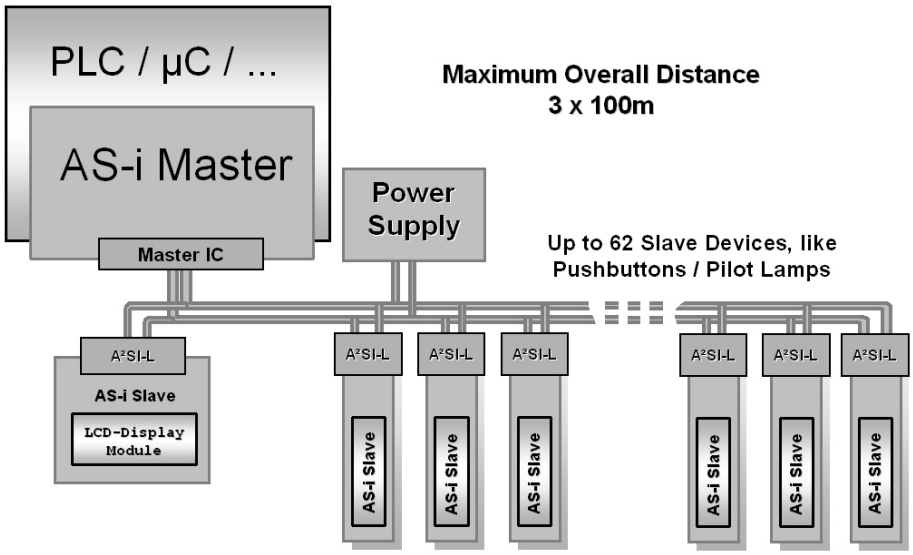
2 Description

AS-Interface is an open worldwide industry standard, IEC 62026-2 and EN 50295 (EU).

The A²SI-Lite 14 (A²SI-L14) and the A²SI-Lite 16 (A²SI-L16)[1] are simplified slave interface ICs, designed for small AS-I slave applications. The device is adapted for low cost devices such as pushbuttons, pilot lamps, simple sensors and small actuators.

A²SI-L Certification Number: 42603
Complete Specification V2.11 compliant

3 A²SI-L14 / A²SI-L16 Network Topology



4 Introduction

A²SI-L is a dedicated interface IC for AS-interface (Actuator Sensor Bus). Besides its special features as described in the A²SI-L Data Sheet[2], the IC is compliant to the Complete Specification AS-interface [1]. This application note refers to both documents and shall support practical issues concerning the application of the A²SI-L circuit. The following specific features are covered:

- Internal status register,
- EEPROM content and EEPROM programming techniques,
- Status indication and security features, and
- Network set-up techniques (address reassignment)

Finally this document illustrates simple application circuits and deals with recommendations concerning necessary external components and PCB design issues.

[1] A²SI-L16 has the same features like the A²SI-L14, provide additional LED and FID Pin

A²SI-Lite 14 / A²SI-Lite 16

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*patent pending

5 References

[1] Actuator Sensor Interface (AS-interface) Complete Specification Version 2.11 Revision 1, 31.1.2002

[2] A²SI-Lite 14 / A²SI-Lite 16 Data Sheet Rev. 2.0

6 Scope

The application hints in this document should be understood as guidelines for designing circuits with A²SI-L. No guarantee can be given for completeness or fully conformity to certain standards. A²SI-L has been designed to comply with IEC 62026-2, EN 50295 and [1]. Since A²SI-L is a component and not a complete system, other components in a system may influence the performance of the whole system. Therefore, system conformity with standards is not the responsibility of ZMD and remains at the customer site.

Recommendations are based on experience with various A²SI-L14 and A²SI-L16 applications as available at the point in time of issuing this document and subject for updating if new information available. However, there is no guarantee that the provided recommendations will lead to a successful application in all cases.

It is recommended also to consult the A²SI-L14/ A²SI-L16Data Sheet [1] for complete and detailed information about full features and properties of A²SI-L.

7 Configuration and Actuator Sensor Bus Operation

7.1. Important Registers

7.1.1. Status Register

Table 1 shows the IC's status register content. The use of status bits S0, S1 and S3 is compliant to the AS-Interface Complete Specification **[1]**. Status bit S2 is not used.

Table 1: A²SI-L14 / A²SI-L16 Status Bits

Status Register Bit	Sx = 0	Sx = 1
S0	EEPROM write accessible	EEPROM access blocked (write in progress)
S1	FID == 0	FID == 1
S2	Static zero	N/A
S3	EEPROM content consistent	EEPROM contains corrupted data

7.1.2. Internal EEPROM

7.1.2.1. General Information

Configuration of the chip is handled through programming of the on-chip E²PROM. ZMD provides a special

AS-Interface Programmer Tool
(Ordering Code: 3000003356)

to ease product evaluation and selection of different operation modes.

One special feature of the A²SI-L is its integrated EEPROM. The non-volatile memory is divided into *user area* and a *firmware area*. The *user area* stores the slave address, along with an ID_Code (ID code extension 1) assigned by the user. If the IC is operating in extended address mode, then most significant bit of this 4-bit data word is used to determine the slave type (A-slave or B-slave; refer to section 7.2 Operation Modes for more detailed information).

The *firmware area* stores the component-specific slave identification codes. Also, flags in this section enable or disable special IC features. By setting the *Program_Mode_Disable* flag in the EEPROM, the manufacturer of AS-i devices can protect the whole firmware area against accidental overwriting.

AS-i Complete Specification compliance note:

In order to ensure full compliance with the AS-i Complete Specification, the *Program_Mode_Disable* flag must be set in the final manufacturing and configuration process before an AS-i slave device is being delivered to field application users.

7.1.2.2. EEPROM Content

For security reasons the EEPROM is divided into several physically separated blocks. However, the user will not notice the internal organization since the EEPROM forms a single memory in terms of its address organization. Table 2 shows the meaning of the sixteen 4-bit wide words.

Table 2: EEPROM Content

A²SI-L14 / A²SI-L16 Internal EEPROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
0	0	A0	Slave Address Low Nibble
0	1	A1	
0	2	A2	
0	3	A3	
1	0	A4	Slave Address High Nibble
1	1 .. 3	(not usable)	Not relevant
2	0	ID1_Bit0	ID_Code_Extension_1
2	1	ID1_Bit1	
2	2	ID1_Bit2	
2	3	ID1_Bit3	
3 .. 7	0 ..3	Logical not implemented - do not access	
8	0	ID_Bit0	ID_Code
8	1	ID_Bit1	
8	2	ID_Bit2	
8	3	ID_Bit3	
9	0	ID2_Bit0	ID_Code_Extension_2
9	1	ID2_Bit1	
9	2	ID2_Bit2	
9	3	ID2_Bit3	
A	0	IO_Bit0	IO_Configuration
A	1	IO_Bit1	
A	2	IO_Bit2	
A	3	IO_Bit3	
B	0	PWM-Enable	Configuration Flags
B	1	PWM_32k_Mode	
B	2	Reserved	
B	3	Reserved	
C	0	FID_Disable	Configuration Flags
C	1	ProgrMode_Disable	
C	2	Watchdog_Active	
C	3	Invert_Data	
D	0 .. 3	Logical not implemented - do not access	
E	0 .. 3	Analogue circuitry trim information Accessible by ZMD only	
F	0 .. 3		

User Area *Firmware Area*

7.1.2.3. EEPROM Write Access

The EEPROM may be programmed in two ways:

1. **Network component set-up: Transmission of the AS-i master calls *Address_Assignment* (ADRA) or *Write_Extended_ID_Code1* (WID1).**

For a functional description of the AS-i master calls, please refer to the AS-i Complete Specification [1]. Both calls are only available at slave address 0x0. By the definition of the master calls it is clear which EEPROM locations must be addressed even if no specific selection is made. The Address_Assignment will effect EEPROM address 0x0 and 0x1. The Write_Extended_ID_Code1 accesses EEPROM address 0x2.

Important: If more than one slave needs to be reprogrammed within a running system, it is recommended to change the slave address or the ID-Code-Extension1 in one slave only at a time. After one slave has been reprogrammed successfully (indicated by the IC status word), the next slave can be reprogrammed.

2. **Invoking *Program Mode*: Transmission of *Write_Parameter* (WPAR) Calls.**

The *program mode* is intended to be used during production set-up of an AS-i slave component at the manufacturer's site. It can be entered only if the slave address was set to 0x0. Note, that no response is generated to the *Enter_Program_Mode* call (as required in the AS-i Complete Specification [1]).

If the *Program_Mode* flag is set, Write_Parameter (WPAR) and Data_Exchange (DEXG) calls have other meanings. In this case the address bits A3...A0 of the master telegrams are used to address one of the sixteen memory locations of the EEPROM (Table 2). Address bit A4 is don't care. The information bits I3...I0 (normally used for output data) carry the data which shall be stored or read from the EEPROM. The Write Parameter initiates a write access. The Data_Exchange is used to read out a specific EEPROM word.

Important: In *Program_Mode* the A²SI-L will generally accept master calls of any slave address regardless of the value of its own address register.

However, any attempt to access one of the not available EEPROM address locations (0x3...0x7, 0xD) through a Write_Parameter (WPAR) or Data_Exchange (DEXG) command or an attempt to reprogram the trim registers (0xE, 0xF) will RESET the circuit.

Any *Write_Parameter* (WPAR) call initializes an autonomous write process within the IC. The status of the write process can be monitored by evaluating the status register of the IC. If bit S0 is set (logical '1') the write process is not finished yet and the programming data is still volatile. If bit S3 is set, the write procedure did not successfully complete either because the write cycle was interrupted or due to an internal error. In order to program the data correctly the write request should be repeated. The status register can be read using the AS-i Master call Read_Status.

7.1.2.4. Recommended EEPROM Access Procedures in Program Mode

As outlined above, the content of the EEPROM can be set-up in *program mode* using master call *Write_Parameter* (WPAR) for write access and *Data_Exchange* (DEXG) for read access for verifying programmed data. As read and write access can not be performed within a single AS-i cycle (master call + slave response), read and write procedures must apply to several rules:

Write Access:

In general, the slave status shall be checked after the master has issued a call that writes into the EEPROM. As long as the slave status indicates that the write process is still going on (S0 = 1, S3 = 0), no further EEPROM accesses should be requested (refer to 7.1.2.1 for AS-i Complete Specification compliance).

An EEPROM programming procedure should be created in consideration of the following steps:

1. Set slave address to zero (if not yet done) by using *Delete_Address* (DELA) call.

2. Enter the program mode by transmitting *Enter_Program_Mode* (PRGM) call.

3. Check the IC's status by using the *Read_Status* (RDST) call (this is recommended prior to attempting any write access to the EERPOM). If status bit S0 = 1, wait at least 23 ms and repeat this step.

4. Perform the write access by transmitting a *Write_Parameter* (WPAR) call.

5. Check the IC's status again (*Read_Status* (RDST) call). If S0 was reset to '0', write cycle finished successfully and next EEPROM location may be accessed.

Read Access:

A *Read_Status* (RDST) call must be performed prior to reading a certain EEPROM address. As the RDST call will reset the EEPROM Read_Pointer, it is a mandatory part of the read procedure. Therefore, it must be applied, also if the slave status information is not intended to be retrieved at that moment. Afterwards, the EEPROM should be read consecutively using the *Data_Exchange* (DEXG) call until the slave responds. In order to select a new address location after a completed read access, a *Read_Status* (RDST) call has to be sent again.

An EEPROM verification procedure should be created in consideration of the following steps:

1. Set slave address to zero (if not yet done) by using *Delete_Address* (DELA) call.

2. Enter Program_Mode by transmitting Enter_Program_Mode (PRGM) call.

3. Make sure that no write EEPROM access is being performed (check the IC's status) and reset EEPROM Read_Pointer using Read_Status call. If S0 = 1, wait a certain time (23 ms is recommended) and repeat this step.

4. Submit Data_Exchange (DEXG) calls until a response is received. The first DEXG will never be answered. Consider also the chance of transmission errors.

5. Continue reading other EEPROM addresses by starting at step (3) again.

7.2. A²SI-L Network Operation Overview

Basically, in AS-I networks the A²SI-L can operate in slave mode only.

The AS-i Complete Specification **[1]** defines an *extended address mode* which permits a maximum of 62 slaves to be operated on a single network. Slaves using *standard address mode* (up to 31 slaves) and the *extended addressing mode* (up to 62 slaves) can still work together in one system. However, it should be noted that *Standard Slaves* will consume the "A" and "B" addresses of the address space which otherwise could be assigned to two slave addresses in extended mode.

To accommodate this enhancement, additional addresses were not simply counted up from 32 to 61, but two new types of slaves (A-type, B-type) were defined**.** A standard slave will be abbreviated with S-slave. A- and B-type slaves share the same 5-bit standard address but can be separated through *Information Bit* I3 of the Master telegram which acts as the select bit (see also AS-i Complete Specification **[1]**). Figure 1 demonstrates the meaning of I3 changes in extended address mode.

Configuration information that defines whether a slave is in extended address mode or not depends on the value of the non-volatile ID-Code register. The AS-i Complete Specification [1] reserves the value 0xA as the ID-Code for slaves in extended address mode. Any other value of the ID-Code register sets the A²SI to standard address mode operation.

Configuration of an A- or B-Slave is done by bit 3 of *ID_Code_Extension_1* register. (user region of the EEPROM, refer to Table 2). If a slave is in extended address mode, the value of this bit is compared to the SEL bit (I3 bit) of the master call. The call is accepted if they match and address register of the slave equals the 5 address bits in the master telegram. It should be noted that bit I3 of a master telegram may represent the bit (SEL) or the inverted select bit (~SEL) depending on type of call.

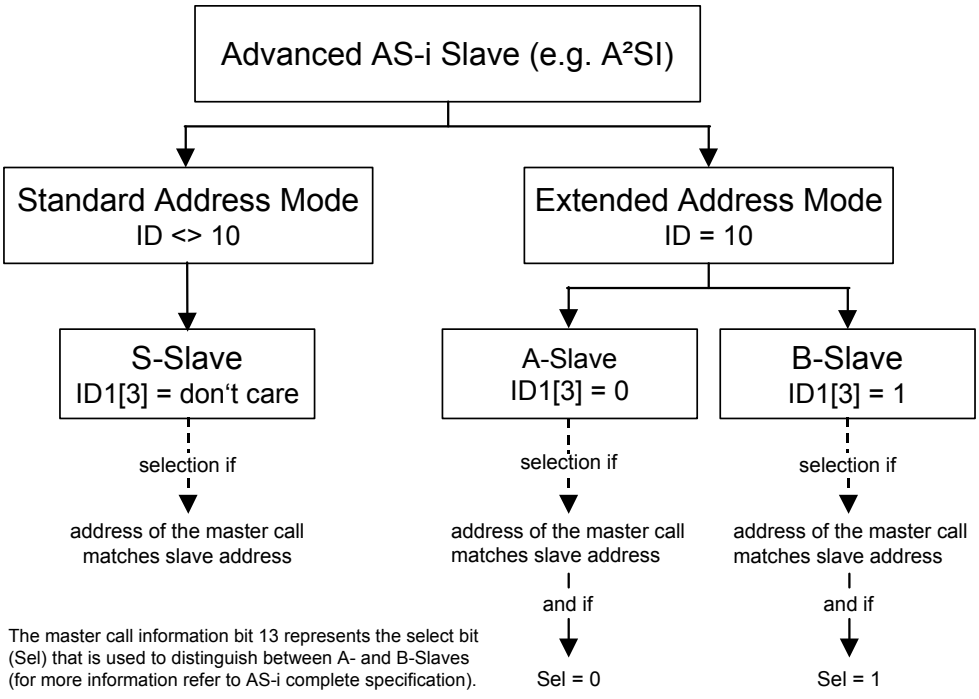

Figure 1: Slave Addressing Modes

There are two exceptions to A-Slave/B-Slave select mechanism:

- It is not used if a slave was programmed to address zero. Slave address 0x0 shall be used for configuration purposes only. Therefore, there is no distinction between standard and extended address mode slaves. Settings of the registers *ID_Code* and *ID_Code_Extension_1* have no impact on slave address 0x0.

- Broadcast calls address all slaves in the network at the same time, no matter whether it is an A-Slave, a B-Slave or an S-Slave.

Bit I3 of a master telegram cannot be used for data communication in Extended Address Mode. Instead, it represents the A-Slave/B-Slave selector (SEL). Depending on the particular master call, bit I3 is equal to SEL or to ~SEL **[1]**.

It is not possible to mix the two addressing modes (*Standard Mode/Extended Address Mode*) on a single slave address (e.g. Standard Slave + B-Slave). Both addressing modes differ in the meaning of the I3 bit. The consequence would be that during DEXCH and WPAR transfers, a situation in which both slaves respond might occur.

7.2.3. The Special Behavior of Slaves with Address = 0

A slave programmed to address 0x0 behaves like an S-slave, regardless of the settings of *ID_Code* and *ID_Code_Extension1* registers.

7.2.4. Recommended Procedure to Change a Slave Address

If the address of a slave shall be reassigned, the user has to make sure that none of following two scenarios can occur:

- The new slave address is identical to the address of another *Standard Slave* in the network.

- The new slave type (A-type, B-type) is identical to another slave's type and both operate at the same slave address (extended address mode only).

Both scenarios will seriously jeopardize the network. There is no way out of such a miss-configuration except through local reprogramming of the slaves.

It is important to know that the A²SI-L will respond to modified addresses or slave types immediately after an appropriate master call (*Address_Assignment, Write_Var_ID_Code*) was received. Although an EEPROM write access will take about 69 ms for an *Address_Assignment* and 42 ms for a *Write_Var_ID_Code* command, the data affects the behaviour of the circuit immediately. The data is first stored in a volatile *Shadow Registers*, which directly control the behavior of the circuit.

Because of above-mentioned reasons, the following sequence of master calls should always be transmitted when slave addresses are going to be changed:

- ***Reset_Slave* (RES) Call.** A slave reset is especially recommended, if the communication watchdog is activated, otherwise a watchdog-reset (refer to chapter 7.2.6.2) could accidentally interrupt an EEPROM write access. A slave reset deactivates the watchdog function temporarily until the first Write_Parameter call has been received. This is because the watchdog is coupled to the status of *Data_Exchange_Disable* flag (Table 2). This flag is set during the initialization procedure of the A²SI and turns the watchdog off. The first Write_Parameter call resets the *Data_Exchange_Disable* flag and enables the watchdog.

- ***Delete_Address* (DELA) Call**. Sets slave address to zero.

- ***Write_Var_ID_Code* (WID1) Call**. A modification of *ID_Code_Extension1* (A-/B-slave selection by ID1_Bit3) must be done prior to any assignment of a new slave address to avoid the second failure scenario described above. This requirement is only relevant for slaves that are intended to work in extended address mode.

- ***Read_Status* (RDST)**. Checks status of EEPROM write process. Repeat this command until S0 = 0 and S3 = 0. Only then, the previous EEPROM write process was successfully completed only as soon as both conditions apply.

- ***Address_Assignment* (ADRA)**. Assigns a new slave address. Note that a new slave address becomes active immediately after a call was received. All subsequent master calls must use this new address and shall not address 0x0.

- ***Read_Status* (RDST)**. Checks status of EEPROM write process. Repeat this command until S0 = 0 and S3 = 0. Only then, the new assigned address has been successfully written into the EEPROM.

7.2.5. EEPROM Data Integrity Check

After any reset (refer to section 7.2.6), the A²SI-L checks the integrity of the data in the user region of the EEPROM. If a preceding write access to the EEPROM did not finish successfully (e.g. because the system was powered down or the slave was reset before the write cycle ended), the IC will detect this immediately after power-on or any other reset. If the integrity check fails, the IC will set status bit S3 to '1' and clear the volatile address register so that the slave will respond to address 0x0 after initialization.

This functionality is only available for the user region of the EEPROM.

A write access to any of the EEPROM addresses is followed by a so-called read-back procedure. The read-back procedure checks the data that was actually stored in the EEPROM against data of the volatile shadow register. If there is a difference, status bit S3 will be set and the failure can be detected by a *Read_Status* call.

7.2.6. IC Reset

7.2.6.1. Operator Introduced Reset

Different events may lead to a reset of the A²SI-L. Following possibilities can be controlled by an operator directly:

- Power-On Reset.
- Reset by Master Call; this reset is available in slave mode only. It can be triggered by sending a *Slave-Reset* (RES) or *Broadcast-Reset* (BR01) master call.

7.2.6.2. Watchdog Reset

Once the communication watchdog was activated (*Watchdog_active_Flag* set and *Data_Exchange_Disable_Flag* reset), it will trigger an unconditional reset as soon as it detects a data communication pause for more than 40 ms. It should be noted that only the reception of a *Write_Parameter* or a *Data_Exchange* call can reset the watchdog. Any other communication between master and slave is not monitored by the watchdog and may therfore cause a watchdog reset too, if the 40 ms time frame is exceeded.

7.2.6.3. Automatic Failure Status Reset

The A²SI-L incorporates counter-measurements against electromagnetic interference to further support the significant security standards of AS-i. In a rough industrial environment, the IC may enter a forbidden logical state caused by a strong electromagnetic pulse. Such forbidden states cannot be invoked through any normal operation but are detected by an independent logic that, eventually, leads the circuit back to a defined state. Once the state machine of the IC has entered a forbidden state, it is very likely that any of the other volatile IC registers may have become disrupted too. To account for this possibility, the A²SI-L performs an unconditioned reset immediately after such failure status was detected.

7.2.6.4. Reset and Initialization Procedure

In any of the above mentioned reset events, the IC will set outputs to a high-impedance state, set the *Data_Exchange_Disable_Flag* to '1', and clear all remaining volatile flags and registers. It will then execute an initialization procedure that copies the content of the EEPROM to volatile (shadow) registers and checks the integrity of the EEPROM user data (refer to section 7.2.5).

7.2.6.5. Over-Heating Shutdown

The chip temperature of the A²SI-L is continuously supervised. If it exceeds the maximum allowable value (e.g. caused by an overload), the circuit will automatically shut down. In this case, the outputs are switched to high-impedance state and the circuit enters an idle state. The idle state is left only after the next power cycle (a power-on reset requires a complete removal of the supply voltage).

7.3. PWM Function

The regular function of the data pins DO0 and DO1 is to send out the corresponding master telegram data of the call Data Exchange. DO0 corresponds to I0 and DO1 corresponds to I1. In addition to that the A²SI-L IC performs a PWM function which is dedicated for the brightness control of LEDs that are interconnected to DO0 and/or DO1, respectively. The PWM function may be enabled by the EEPROM flag PWM_enable.

Table 3: PWM specification of Outputs: Pins DO0, DO1

Intensity of LED	**"Write Parameter" command from Master [1]**			**PWM Frequency 1 / t_{PWM}**	**Pulse duty ratio [2] t_{on} / t_{PWM}**
	P2	P1	P0		
100.00%	Select DO0 or DO1	1	1	DC (default)	16/16
50.00%	Select DO0 or DO1	0	1	125Hz/32kHz	8/16
25.00%	Select DO0 or DO1	1	0	125Hz/32kHz	4/16
12.50%	Select DO0 or DO1	0	0	125Hz/32kHz	2/16

[1] The write parameter call is used to control the intensity of LEDs that are interconnect to the data output pins.
[2] Pulse/duty ratio is defined as the quotient ton / tPWM

The PWM Frequency can be selected by the EEPROM bit 1 of EEPROM address 0xB between 125Hz (bit-value = 0) and 32kHz (bit-value = 1).

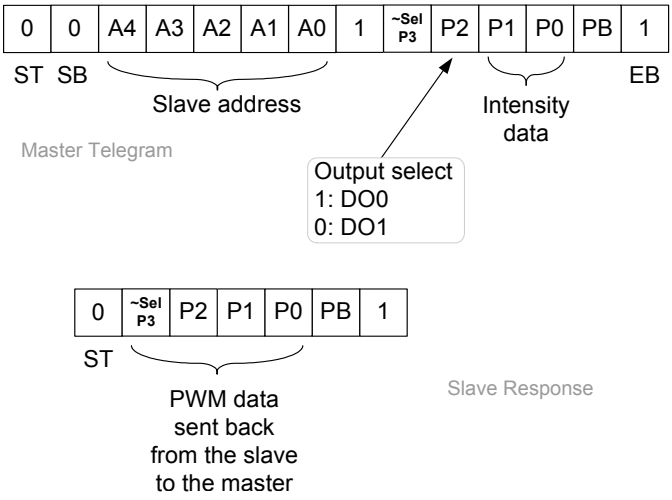

Figure 2: PWM control

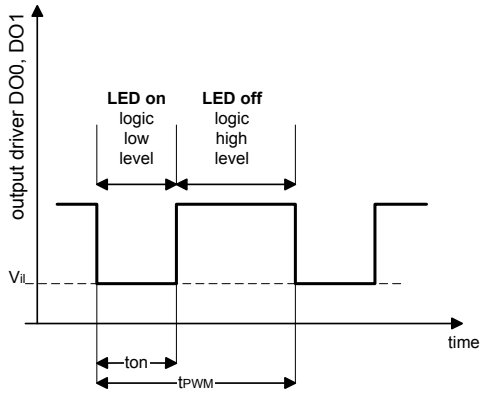

Figure 3: PWM timing diagram

Provided that a lit LED is caused by a logic low level output signal of the related data pin brightness of the LED can be controlled by the master call *Write Parameter* as shown in Figure 2.

After a *Write Parameter* call has been received the pulse duty ratio will be effective after the slave response has been sent. The default duty pause ration is 100% which is set after the initialization phase of the IC automatically. Figure 2 shows the telegram structure of the *Write Parameter* call. and the related slave response data.

7.4. Status Indicator LED (only A²SI-L16)

The LED output is only available at the A²SI-L16 and operates as status indicator output.

The LED operates as a status indicator like implemented in the definitions of the AS-i Complete specification **[1]**. The LED can be on or off, where *LED off* corresponds to *logic high level* at the LED pin (*LED_OUT*). Vice versa *LED on* corresponds to *logic low level* on *LED_OUT*. The LED will display the following status information:

- LED Off:
  - **Communication ON:** The slave can respond to DEXG master calls if its *data exchange disable flag* (*DATAEXCHG_DIS*) has been cleared.
- LED Constant On:,
  - **Communication OFF:** After an IC reset, the data exchange disable flag (DATAEXCHG_DIS) is set and causes the LED to become constant on.

- LED Flashing (2Hz):
    - **Periphery Fault**: In case of a periphery fault (logic high at FID), the LED flashes with a frequency of 2 Hz. Since the FID signal has higher priority than the *Communication OFF* state, the LED will remain flashing even if the Communication is off (*data exchange disable flag* is set).

7.5. Fault Indication Input FID (only A²SI-L16)

The fault indication input FID is a digital input that is dedicated for a periphery fault messaging signal. The S1 status bit is equivalent to the FID input signal. A FID transition will be occur at S1 with an certain delay because of a synchronizer circuit is put in between.
In case of the 14 pin IC version (A²SI-L14) the FID input is not available. The slave module manufacturer has to disable this function by programming a related EEPROM cell (EEPROM bit 0 of EEPROM address 0xC). A disabled FID pin function shall be equivalent to a logic low input signal at an enabled FID pin. Therefore the status bit S1 is always cleared if an IC is having a disabled FID pin.

8 Application Info

8.1. Pin Description

Table 4: Pin List

A²SI-L14	A²SI-L16	Name	Type	Description	Remarks
1	1	ASIPOS	INOUT	TO BE CONNECTED TO THE AS-I-LINE ASI+ VIA REVERSE POLARITY PROTECTION DIODE	
2	2	ASINEG	INOUT	TO BE CONNECTED TO THE AS-I-LINE ASI-	ASIN should be interconnected with the 0V-pin. Route from ASI- to ASIN and then to 0V and GND.
3	3	Test1	In/OUT	Test mode input output	Always connect to GND
4	4	Test1	IN	Test mode input	Always connect to GND
5		FID	IN	Input peripheral fault indication	Refer to DI2
6	5	DI2	IN	Input of data D2	Contains an internal pull-up transistor, The input voltage is internally clamped to 5V (consider higher input current if V_{IN} > 5V)
7	6	DI3	IN	Input of data D3	Refer to DI2
8	7	OSC2	INOUT	Crystal oscillator / external clock input	The x-tal oscillator does not require additional electronic components.
9	8	OSC1	IN	Crystal oscillator (16 MHz x-tal)	
10	9	DO1	OUT	Output of data D1	Open-drain output
11	10	DO0	OUT	Output of data D0	Open-drain output
12		LED	OUT	Output LED "AS-i-Diagnosis"	Open-drain output
13	11	GND	SUPPLY	Digital IO ground	NOTE: GND and 0V must be connected externally by low resistance and low inductance wiring.
14	12	CAP	INOUT	Regulator output	To stabilize the 5V voltage
15	13	0V	SUPPLY	Common 0V for all IC-ports except ASIP/ASIN (usually to be connected to the AS-i-line ASI-)	Must to be interconnected with GND. This interconnection should be as short as possible to avoid voltage drops between the pins.
16	14	V_{IN}	SUPPLY	Input of the power supply block	has to be connected behind the decoupling inductor

8.2. External Components

Table 5: A²SI-L14 / A²SI-L16 External Components

Pin 1 to pin 2 or Pin to external node	**External components**	**Remarks**
Vin to 0V	10µF electrolyte capacitor in parallel 100 nF ceramic capacitor	Higher value of the electrolyte capacitor is recommended if there are strong load current changes.
CAP to 0V	1µF electrolyte capacitor in parallel 100 nF ceramic capacitor	
OSC1 to OSC2	16.000 MHz standard x-tal, dedicated load capacitance approximately 7 ... 15pF	Calibration tolerance < ±60ppm
LED to Vin	Pull-up resistor typical 100 kohm	If no LED is being connected and if the PCB is causing a high parasitic capacitance at the LED pin
DI2, DI3 to Vin	Pull-up resistor (10 kohm …100 kohm) recommended	In order to avoid EMC problems
ASIPOS to V_{IN}	9 mH…18 mH inductor, dependent from the slave type alternatively use the electronic Inductor solution from ZMD	Refer to Table 7 To divide the slave circuit from the AS-I line.
ASIP to ASIN, 0V, GND If applicable U_{IN} to ASIN, 0V, GND	Suppressor diode 39V, 0.5W	To comply with the AS-i Complete Specification **[1]**, a reverse polarity protection diode must be applied.

	Slave (stand.)	Slave (stand altern.)	Slave S-X.A	Slave S-X.A (altern.)
R’	>8kΩ	>8kOhms	>16kΩ	>16kΩ
C’	<100pF	< 70pF + (L - 6 mH) * 10 pF/mH	<50pF	<35pF + (L’-12mH)*2,5pF/mH
L’	>9mH	6 ... 9 mH	>18mH	12...18mH

*Table 6: A²SI-L External Inductor concerning Complete Specification **[1]***

8.3. Application Circuits

Following figures show typical application cases of the A²SI-L IC.

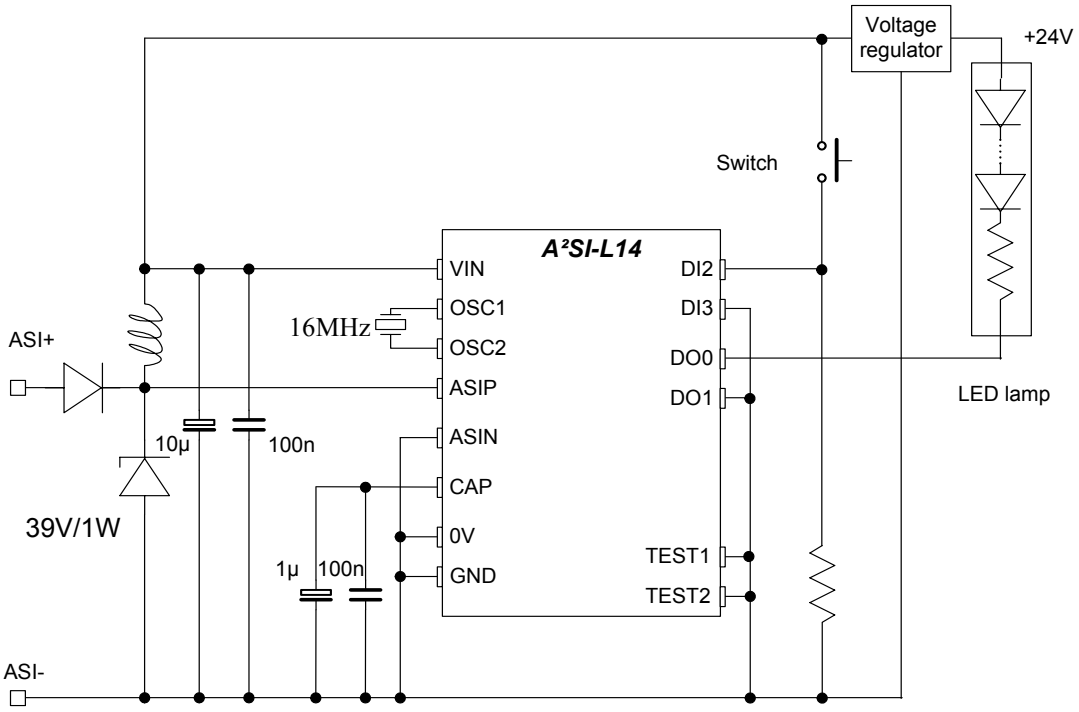

Figure 4: Application circuit for a slave application A²SI-L14

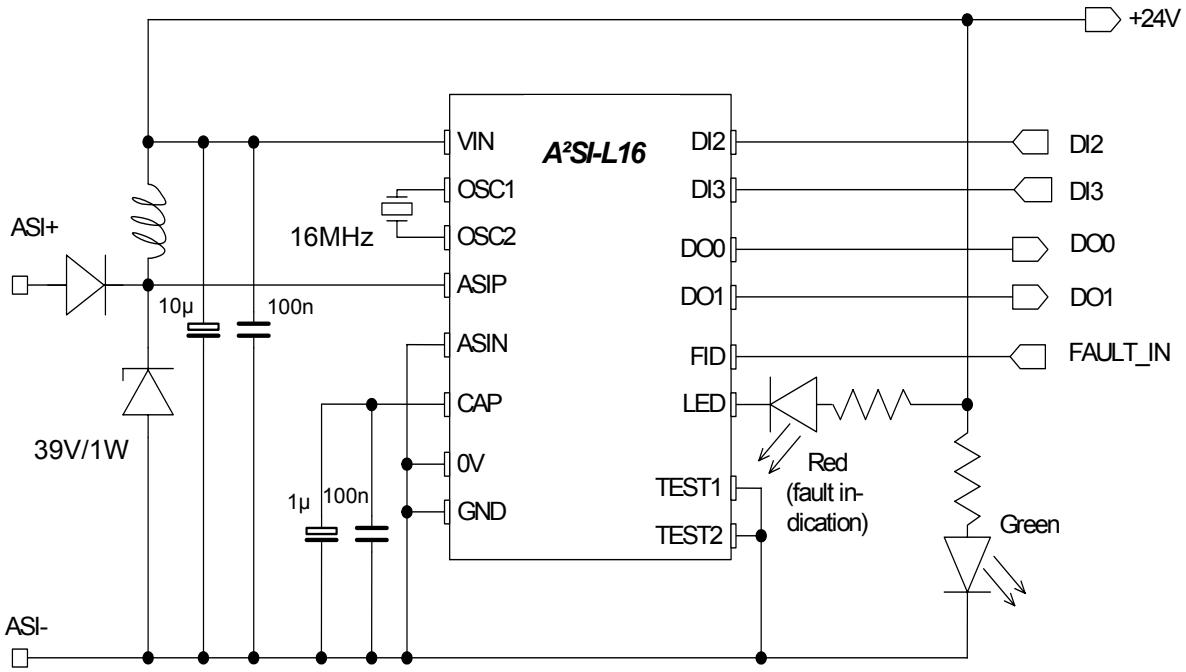

Figure 5: Application circuit for a slave application A²SI-L16

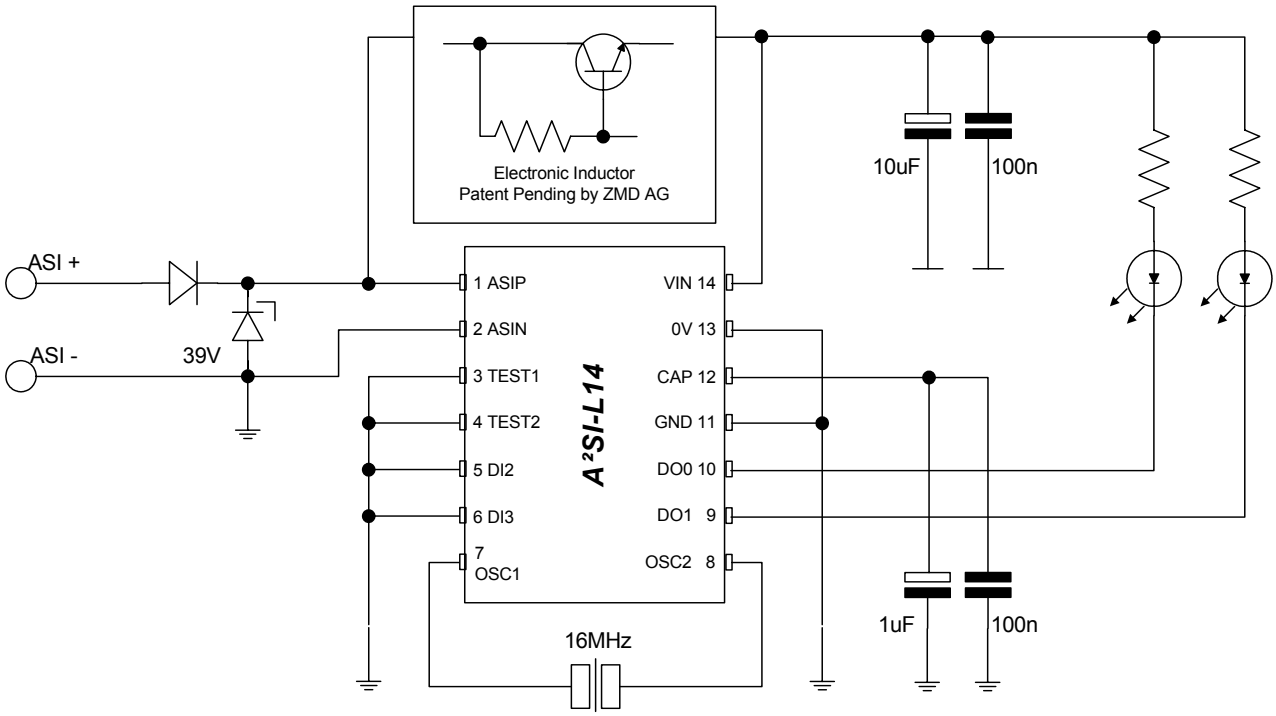

Figure 6: Application circuit for a slave application with electronic Inductor*

ZMD provides an optional application for a bipolar (GND free) electronic inductor to replace a mechanical coil with some inexpensive electronic parts. This solution save costs, board space and will be more resistant against mechanical vibrations. This inductor provides a supply current up to 90mA to Vin and the connected circuit, respectively.

ZMD AG provides a license to ZMD AS-Interface IC customers free of charge.

For further information, please contact:

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* patent pending

8.4. PCB Design Recommendations

To assure correct operation of the IC, the following facts should be considered when designing a PCB for an A²SI-L application:

- Interconnection between the crystal and IC should be as short as possible and large parasitic capacities at the pins should be avoided. Ensure that no parasitic capacitance accrues between the XTAL lines and Power/GND lines (parallel layers).
- The 0V and GND pins must be directly connected. The decoupling capacitors between CAP and GND/0V must be placed as close as possible to the CAP and 0V pin, respectively.
- The ground node of the external slave electronic circuitry (which is controlled by the IC) should be directly connected to the ASIN pin (the wire should not pass through to pin 0V and then to pin GND). It should have a low ohmic resistance and a low inductance. Use a star-shaped routing structure for GND, beginning from the GND pin.
- The connection of the ASINEG pin to the 0V pin should not run via the GND pin. This wiring resistance may have some inductance (maximum value not yet defined). The optimal routing is ASI- (Input) to ASINEG, then to 0V, and then to GND.

9 Application Support

9.1 AS-International Association

Documentation and promotional materials as well as detailed technical specifications regarding the AS-Interface Bus Standard are available from:

AS-International Association
Contact - Rolf Becker
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http://www.as-interface.net

Refer to the Association's website here above for contact info on nine local AS-Interface associations which provide local support within Europe, in the US and in Japan.

9.2 ZMD

A²SI-L14 / A2SI-L16 device related application support requests can be addressed to asi@zmd.de.

9.3 ZMD Application Support Partners

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10 Sales Contacts

10.1 ZMD Sales Contacts

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